REMARKS

I. Claim Rejections

A. 35 USC § 112

Claims 1 and 6 have been rejected under 35 USC 112, second paragraph, as being "indefinite", based on the inclusion of the terms "substantially continuously updating" and "substantially continuously updated", respectively.

Each of claims 1 and 6 has been amended by deleting "substantially" to overcome this rejection.

B. 35 USC § 102 (e)

Claims 1 – 25 have been rejected under 35 U.S.C. § 102 (e) as anticipated by Safavi et al. (US Pub. No. 2003/0123579 A1).

It is noted that claim 26, added by amendment of 10/28/04 was not considered by the Examiner.

The Examiner relies principally on page 5, sections [0088] – [0090] of SAFAVI for concluding that the independent claims 1 and 11 are "anticipated". Additional text and/or drawing figures are also noted by the Examiner in rejecting independent claims 17 and 23, along with specific dependent claims including claim 10. Sections [0033], [0084] and [0091], as well as Fig. 3, Fig. 12, Fig. 13 A & B and Equation 1-2 (page 2) are specifically relied on for "anticipation" of these latter claims and the remainder of the claims.

2. The SAFAVI '579 Published Application relied on Under 35 U.S.C. 102 (e) Lacks Numerous Elements of This Invention

The rejection under § 102 (e) based on SAFAVI is respectfully traversed and withdrawal of that rejection is requested for the following reasons.

In the rejection of each of the 25 claims, the Examiner merely states "In respect to claim x, Safavi teaches ---". The Examiner then proceeds to copy the entire element by element language of each respective rejected claim and states

all such elements are found in SAFAVI. The Examiner's "position" concludes, for each claim, with a brief "Note" identifying one or more drawing figures, equations and/or "sections" of the specification of SAFAVI. With the exception of rejected claim 10, there is no element by element comparison of any of the claims to any of what is described or illustrated in SAFAVI.

In order for a reference (patent) to anticipate a claim under 35 U.S.C. § 102 (e), It is fundamental that "the (entire) invention", that is, each and every element of the rejected claim(s), must be described in the cited reference. This principal has been described in CAFC decisions which are set out in the MPEP as follows (regarding "anticipation" under §102 of claims).

"Thus, in order to anticipate a claim, the reference must teach every element of the claim. That is,

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. V. Union Oil Co. of California, 814 F2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).".

"The identical invention must be shown in as complete detail as is contained in the ----claim." Richardson v. Suzuki Motor Co., 868 F2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). ".

Contrary to what the MPEP (and the law) requires, the Examiner is relying on a reference (SAFAVI) from which the Examiner has picked out a few paragraphs of text which may disclose some similar structural elements but fail to disclose "all elements" (the subject matter) of any complete rejected claim.

As noted above in the Richardson case, the law requires that "the identical invention", be disclosed to support a §102 rejection.

With respect to claim 1, the Examiner relies on "sections [0088] – [0090] in SAFAVI.

The text of those sections of SAFAVI reads as follows:

"[0088] An alternative is to use a hybrid "register-exchange and trace-back" method. In this method, the bit sequence is kept for a certain number of stages n, then stored into memory. Eventually, instead of keeping the up-low bit in memory to find the correct survivor path, segments of

decoded bits are kept for each path. In the trace back stage, after finding the survivor state, decoded bits of the preceding n stages can be accessed. The trace back for every state need not be done. After finding one state and picking the n decoded bit sequence, the method can jump to the n.sup.th preceding stage (present stage-n). This approach shares the effect of trace back cycles over n bits, so that the portion of trace back cycles on total cycles/decoded bit will be reduced from 18 to 18/n, assuming that trace back requires 18 cycles per iteration.

[0089] The number of cycles required in stage 3 can also reduced, as the up-low bits do not need to be packed, and the survivor path does not need to be stored at every iteration but only in every n.sup.th iteration. One possible drawback of this approach can be found at stage 4. The re-ordering (re-shuffling) stage is more time consuming due to re-ordering of decoded bit registers.

[0090] In one embodiment, the optimum n is 16, in which a single register per state is used for decoded bits. Up to a 35% reduction in the number of cycles required can be realized. FIG. 12 shows the hybrid method using a single 16 bit register for a decoded bit sequence of each state. Note that in order to keep track of the survivor path, a way of recording the previous state at every n stage is needed. Due to the reordering of this register between stages, the initial state of each register at first stage is not known. It may not be sufficient to include only a single up-low bit to specify the previous state. Therefore 8 bits (MSB) of this register can be assigned to the index of the previous state, that is, 256 possible states. Although the need for a previous state index decreases n from 16 to 8, it still reduces the total cycles by about 30%.".

It is respectfully submitted that the description of SAFAVI's system above does not include (see rejected claim 1) any "means for selecting a desired trellis state path from the antecedent trellis states" or "means for continuously updating the desired trellis state path at each new trellis branch" (rejected claim 1).

Independent claim 11, which is said to be rejected "for the same reasons as claim 1", relates to a method which includes method steps including "selecting" and "continuously updating" steps that correspond to the apparatus elements noted above in claim 1 which are not found in the cited sections of

SAFAVI.

Dependent claim 2 has been rejected based specifically on the SAFAVI text in section [0090] and the drawing of SAFAVI Fig. 12. That text is set forth above but no relationship has been shown in the rejection between that text and the added elements of claim 2, i.e.,

"means for performing an all-path traceback through the trellis; and

means for performing an all-path forward trace through the trellis.".

It is respectfully submitted that these elements of claim 2, as well as the previously noted elements of claim 1, are not disclosed in the cited sections of SAFAVI.

Similarly, the rejection of claim 3 (which is dependent on claim 2) relies on section [0090] but there is no mention in that section of "means for continuously identifying the desired trellis state path at each new trellis branch with a forward trace pointer ----" as required by claim 3.

Dependent claims 4 – 9 all depend from claim 3 and/or intervening claims and therefore distinguish over SAFAVI at least to the same extent as claims 1, 2 and 3 as noted above.

Claim 10, which is dependent on claim 2, has been rejected on the basis of the same sections [0088 – [0090] plus sections [0084] and [0033].Those additional sections read as follows:

[0033] FIG. 3 illustrates an rDSP chip 200 in greater detail, showing: the RISC processor 104 with its associated instruction cache 202 and memory controller 204; an RC array 102 comprising an 8-row by 8-column array of RCs 206; a context memory 208; a frame buffer 210; and a direct memory access 212 with its coupled memory controller 214. Each RC includes several functional units (e.g. MAC, arithmetic logic unit, etc.) and a small register file, and is preferably configured through a 32-bit context word, however other bit-lengths can be employed.

[0084] In order to optimize the mapping, the execution flow is discussed. As shown in FIG. 11, the total execution cycle in trace forward is 52 cycles. Stage five will be executed once per block, so the portion of its execution load per bit is negligible. The trace back stage takes 18 cycles per bit. There will be an overhead of about 10% for

index addressing and loops. Thus, employing the mapping shown in FIG. 11 will result in about 77 cycles per decoded bit.

The Examiner has also associated "frame buffer 210" in the text above with the recitation of "a buffer memory" in claim 10.

In addition, the Examiner associated the text of section [0084] with the element "means for reading the data from the buffer memory unit during the following epoch and sending it to the all-path traceback unit", none of which can be seen to be described in the cited sections [0084] or section [0033].

Thus, there are significant additional elements recited in claim 10 which are not found in the cited sections of SAFAVI.

Dependent apparatus claim 5 and dependent method claim 12 each have been rejected on the same basis as their respective parent claims 3 and 11, respectively) and, further in view of section [0091]. That section reads as follows:

[0091] In a typical Viterbi decoder, depending on the data frame size and the memory availability for each specific implementation, the decoder processing can be performed on the received sequence as a whole, or the original frame can be segmented prior to processing. The latter case would require a sliding window approach in which state metrics computation of segment (window) i+1 will be done in parallel to the trace back computation of segment i as shown in FIG. 13 (i.e. overlap between windows).

No relationship is perceived between the language of section [0091] above and any of the detailed language of either claim 5 ("first pointer", "second pointer", "epoch", "survivor memory depth") or claim 12 ("epoch boundaries", "traceback interval", "survivor memory depth") and those claims are therefore submitted to be patentable, as well as their respective parents.

All of the remaining claims, 13 – 25 are said to be "rejected for the same reasons as claim 10".

It is noted that claims 13 – 16 are method claims dependent from claim 12 and are not related to dependent apparatus claim 10. Claims 13 – 16 are submitted to be patentable for the same reasons as claims 11 and 12.

Claims 17 and 23 are independent apparatus claims while apparatus claims 18 – 22 are dependent on claim 3.

Claim 17 recites particular "pointer" relationships that have nothing to do with claim 10 or with the sections of SAFAVI cited against claim 10 and is therefore submitted to be patentable over SAFAVI.

Independent claim 23, as well as dependent claims 24-25, also recite in significant detail, pointer relationships different from claim 10 and different from the cited portions of SAFAVI, which are submitted to make claims 23 – 25 patentable over SAFAVI.

Claims 18 – 22, which distinguish over the cited art for the same reasons as the claims (1 – 3) from which they are dependent, recite increasingly detailed attributes of "pointers" which have not been identified in SAFAVI. As such, the substantial, detailed recitations of claims 18-22 distinguish those claims over the cited reference.

CONCLUSION

Claim 26, added by amendment of 10/28/04 to this application was not considered by the Examiner. However, it has been amended similarly to other claims to which an objection was raised in order to make it allowable.

In the Office Action, there is no element by element comparison of the language of the claims to what is described or illustrated by Safavi.

The language of the independent claims 1, 11, 17 and 23 is respectfully submitted to distinguish such claims over the cited reference. In addition, substantial language in each of the rejected dependent claims as pointed out above is not seen to be found in the cited reference.

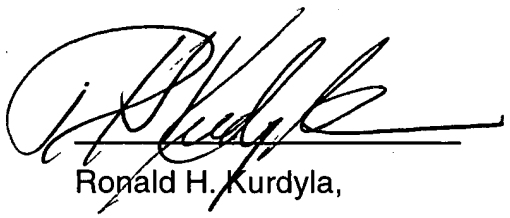
In order to anticipate a claim, the reference must teach every element of the claim. That is,

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. V. Union Oil Co. of California, 814 F2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).".

It is respectfully submitted that the claims of this application are not anticipated by SAFAVI.

In view of the foregoing amendment and REMARKS, reconsideration and withdrawal of all of the rejections and allowance of all pending claims 1 –26 are respectfully requested.

Respectfully submitted,



Ronald H. Kurdyla,
Attorney
Registration No. 26,932
609/734 – 6818

Patent Operations
Thomson Licensing Inc.
P.O. Box 5312, 2 Independence Way
Princeton, New Jersey 08543
April 24 , 2006

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in a postage paid envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22301-1450 on the date indicated below.

Date: 4-24-06 **Signature** Karen Scalancy